IN THE CLAIMS

Claims 1-9 (Canceled).

10 (Previously Presented). An article comprising one or more machine-readable storage media containing instructions that when executed enables a processor to:

receive a video stream having at least a first type of frame and a second type of frame; and

process the first type of frame using a first error resilience technique and the second type of frame using a second error resilience technique, wherein the first error resilience technique comprises applying resynchronization markers to the video stream at a selected interval and the second error resilience technique comprises applying resynchronization markers at an interval different from the selected interval such that the second error resilience technique replaces a bit pattern for the second type of frame with a bit pattern of shorter length.

11 (Original). The article of claim 10, wherein the instructions when executed enable the processor to process a P-type frame using the first error resilience technique.

12 (Original). The article of claim 11, wherein the instructions when executed enable the processor to process a B-type frame using the second error resilience technique.

13 (Original). The article of claim 12, wherein the instructions when executed enable the processor to process the B-type frame using a simpler error resilience technique than the P-type frame.

14 (Original). The article of claim 13, wherein the instructions when executed enable the processor to insert resynchronization markers in the video stream at a first pre-selected interval for the B-type frame and at a second pre-selected interval for the P-type frame, wherein the first pre-selected interval is longer than the second pre-selected interval.

15 (Original). The article of claim 10, wherein the instructions when executed enable the processor to process the first type of frame using a first error concealment technique and the second type of frame using a second error concealment technique, wherein the first error concealment technique is different from the second error concealment technique.

16 (Original). The article of claim 10, wherein the instructions when executed enable the processor to insert fewer error resilience bits into the video stream for the B-type frame than for the P-type frame.

17 (Original). The article of claim 10, wherein the instructions when executed enable the processor to perform variable length coding on the B-type frame.

18 (Original). The article of claim 10, wherein the instructions when executed enable the processor to apply resynchronization markers to the video for the B-type frame.

Claims 19-33 (Canceled).